

CleanQ: a lightweight, uniform, formally specified interface for intra-machine data transfer

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Abstract

We present *CleanQ*, a high-performance operating-system interface for descriptor-based data transfer with rigorous formal semantics, based on a simple, formally-verified notion of ownership transfer, with a fast reference implementation.

CleanQ aims to replace the current proliferation of similar, but subtly diverse, and loosely specified, descriptor-based interfaces in OS kernels and device drivers. *CleanQ* has strict semantics that not only clarify both the implementation of the interface for different hardware devices and software use-cases, but also enable composition of modules as in more heavyweight frameworks like Unix streams.

We motivate *CleanQ* by showing that loose specifications derived from implementation lead to security and correctness bugs in production systems that a clean, formal, and easily-understandable abstraction helps eliminate. We further demonstrate by experiment that there is negligible performance cost for a clean design: we show overheads in the tens of cycles for operations, and comparable end-to-end performance to the highly-tuned *Virtio* and *DPDK* implementations on Linux.

1. Introduction

CleanQ is a uniform operating system interface for transferring bulk data, which abstracts from and unifies a wide variety of descriptor-based data transfer interfaces used by both software and hardware in a modern OS.

Queues based on descriptor rings are pervasive in OS code for moving data between processes, hardware devices like network adaptors, kernel and user space, etc. Despite this there is a wide range of different queue interfaces and implementations (even within a single OS). So-called standard interfaces to queues, where they exist, are typically specified informally using a reference implementation in C.

This leads to a serious problem, which we elaborate on in Section 2. Implementations cannot be reused (since the semantics are subtly different), and thus implementation *bugs can recur* (and do) when a new queue is built. The lack of clear semantics mean that bugs also arise due to *inappropriate use* of a given descriptor queue, by a client programmer who may not understand its subtleties, and also make it *hard to compose* code modules which operate on queues of data, as is possible with Unix Streams or other I/O frameworks. Without a formally sound description of a queue’s behavior, it is *impossible to reason* about the correct behavior of the OS which uses them. Finally, a lack of uniformity is a lost opportunity to *build and apply standard tools* for debugging, validating,

profiling, and monitoring such queues at runtime, making OS development more difficult and time-consuming.

CleanQ addresses these problems not by simply proposing yet another queue interface, but starting from a *provably sound formal specification* (presented in Section 3) of how a descriptor queue should behave. This gives clear guarantees to clients of a queue (whether it be a device driver or an inter-process communication system), and also states clear obligations on the code that implements an end-point of the queue.

The specification is strict, and so the chance of subtle mismatches between the expectations of client and implementation are eliminated. It allows for full concurrency between actors, such as a driver process and a network card. It also subsumes the memory model in use: the client of a CleanQ queue does not need to be concerned about weak consistency or non-coherent memory in order to write correct, portable code to use it. However, CleanQ focuses purely on the data plane interface, leaving flexibility to system designers in how such queues are instantiated and provisioned.

From the specification, we then proceed to a C interface which captures it. This interface is highly general. In Section 4 we describe it and demonstrate its generality with a number of implementations we have built behind it, for network cards, storage adaptors, and inter-process communication. Moreover, the CleanQ C interface composes: we also describe CleanQ modules that provide loopback, debugging and network stack functionality.

Finally, we evaluate the overhead of using our CleanQ implementation modules on Linux and a microkernel-based research operating system in Section 5 to show both performance and portability. We show that, despite the strict semantics and highly specified, uniform interface, CleanQ is cheap: it is comparable to *Virtio* and *DPDK* in operation latency and imposes less than 1% overhead for set/get operations using *Memcached* [17].

2. Background and Motivation

CleanQ is a formalization of descriptor rings. Rings of descriptors are a fairly pervasive technique for transferring data between end-points (software processes or threads, GPUs, address spaces, hardware I/O devices, virtual machines, etc.) in a modern OS. Each descriptor refers to a region of memory (usually elsewhere) plus some metadata, including which end of the communication “owns” the data (and metadata). The Linux kernel alone has at least 6 different descriptor queue implementations, not including hardware-specific I/O queues

for network and storage devices.

Descriptor rings work well because they highly decouple sender and receiver: sending data between a user process and a high-performance network adaptor using Intel’s DPDK [28], for example, doesn’t require either side to touch payload data as part of the transfer, and in the common case requires no synchronization between sender and receiver. In such drivers, interrupts and hardware register access is only used for coarse-grained synchronization at low load levels; for the most part each side of the communication can proceed in parallel without explicit coordination.

However, while the *technique* of descriptor rings is almost universal, there is little consensus on what a given ring should look like. A great number of software interfaces, libraries and ‘standards’ have been proposed over time (e.g. [16, 19, 43, 1, 32, 22, 3]) all of which are variations or enhancements of the same basic theme. Moreover, every new high-performance I/O device adopts a different descriptor format for its I/O queues, including devices from the same vendor (e.g. [39, 24, 26, 27, 25, 4]).

2.1. The Continuing Emergence of Descriptor Bugs

This proliferation of implementations is often for good reasons: queue implementations (whether communicating between processes or between software and hardware devices) have different requirements in how they are constructed and set up, metadata that may need to be passed with each buffer, and additional, implementation-specific semantics associated with enqueue and dequeue operations. Examples are Virtio [43] for buffer transfer between host and virtual machines, SKBuffs[35] in the Linux network stack or mbufs in DPDK [28]. However, the proliferation of implementations combined with the difficulty of getting memory semantics right leads to a steady stream of serious bugs, ranging from performance problems to critical security vulnerabilities.

For example, the Virtio framework used in the QEMU emulator and the KVM virtual machine monitor has allowed a malicious guest to break security by inserting more requests than the size of the queue [13]. Changing the queue parameters in Virtio has caused the hosting QEMU process to crash [41]).

Worse, these bugs have not only been appearing for a long time – they continue to appear [7, 8, 9, 40, 12, 10, 11, 13, 15, 14, 41, 6] in Linux and Android (and, we suspect, other system software). A new class of “double-fetch” bugs/vulnerabilities have recently appeared [46] whereby data is fetched twice but changed by another party in between. All these bugs ultimately boil down to production code making incorrect assumptions about when and how memory can be accessed safely by one side of a descriptor queue-based channel: when it is safe to reuse a buffer, when an endpoint can safely enqueue another buffer, etc.

We argue the main reason this problem is not going away is the prevalence of *specification by implementation*: The documentation—where it exists at all—is written in English

and not formally specified. For example, consider the virtqueue mechanism in Virtio [43] for transferring data between a device driver and a virtual device.

A virtqueue consists of (1) a *descriptor table* specifying which buffers a driver is using for its device, (2) an *available ring* containing descriptors offered to the device, and (3) a *used ring* containing buffers processed by the device and returned to the driver.

While the specification makes it clear that buffers available to the programmer are on one of the two rings, the corner-cases (such as adding a descriptor twice to a ring) are undocumented. Programmers are ultimately advised to read the code. To make things worse, Virtio has two different queue interfaces—one for the host and one for the guest—having slightly different semantics (e.g. a memcopy on the host side).

2.2. Lack of Portability and Reuse

A further consequence of specification-via-implementation is that correctness often depends on a particular memory model. The combination of program operations and fences/barriers required for correct operation is not at all obvious from the documentation, and is different for different processor architectures. For example, when a device driver enqueues a buffer, it first writes the buffer contents, then the descriptor, and finally updates the head pointer of the ring buffer to inform the device that there is a new descriptor. On a machine with a weak memory model, these operations can be reordered and the device notified before the descriptor is written to memory.

Consider, for example, invoking a Virtio [43] or fbuf [16] based queue between two cores: an Intel x86 machine implements Total Store Ordering [44], leading to a relatively simple implementation: if a thread performs two writes w_1 before w_2 , another thread that observes w_2 will also have observed the effect of w_1 . Implementing buffer transfer for x86-TSO or similar models, it suffices to ensure correct write ordering.

However, machines with weak memory consistency like ARMv7, ARMv8, or IBM Power [18] allow considerable relaxation in the visibility order from a given core: any load, store, *or* atomic instruction can be extensively reordered around other loads and stores. A correct queue therefore requires tricky use of barrier and fence instructions.

Moreover, given the number of descriptor queue implementations in a typical OS, it is surprising and disappointing that generic functionality cannot be shared among implementations, nor can implementations *compose* efficiently into a pipeline, in the manner of more heavyweight data transfer frameworks like Streams in AT&T [42] and Plan 9 [38], or the protocol modules in the x-Kernel [23].

2.3. CleanQ

The duplication of code and continuing stream of new bugs in ad-hoc descriptor queues led us to develop CleanQ, a formally-

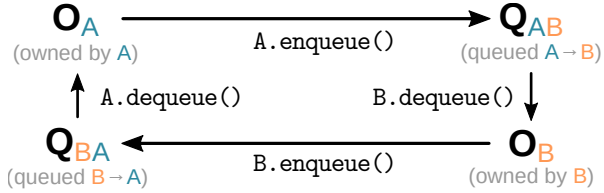


Figure 1: Ownership transfer

specified data transfer model for descriptor queues with an associated C-language interface.

To the best of our knowledge, CleanQ is the first practical, formally-specified, general-purpose descriptor ring abstraction, and we show that the generality and strict semantics of CleanQ come with negligible performance penalty compared with poorly-specified (but well-implemented) subsystems in production use.

By decoupling rigorously defined data transfer semantics from implementation, CleanQ allows clients and implementations to be developed and tested separately with much greater assurance of correctness. CleanQ is a specification and not an implementation, thus leaving orthogonal issues like metadata, setup, and additional semantics to the implementation while adhering to a single common model for data transfer.

CleanQ is highly general: it can express a variety of hardware descriptor queues as well as communication channels between processes in an OS. We demonstrate this functionality by later implementing, among other things, a debugging module which is transparent to a CleanQ queue but applies rigorous online checking of its arguments.

CleanQ is *not* “yet another queue implementation”, nor is it a bug-finding technique for existing implementations. Moreover, our goal is not to build a formally verified system (such as seL4 [31] or CertiKOS [21]), but rather a sound basis for reasoning about the system and its behavior and having clearly defined semantics. CleanQ is an example of how a useful subset of the benefits and guarantees of full-stack verification can be practically introduced into existing systems in a portable and incremental manner

A concise, formally-sound model such as CleanQ is essential to the development and proof of formal systems software, but it is just as important for non-verified systems such as Linux. As long as the implementation of a CleanQ module adheres to the specification, we can guarantee properties proved on the formal model.

3. Model

The interfaces we consider (e.g. `virtio`) all transfer data in *buffers* (packets, VM pages, disk blocks, etc.) between *processes* (including software processes, device drivers, hardware devices, etc.). The copy itself is simple (for a zero-copy implementation, it is completely absent). The principal difficulty is the bookkeeping: When can a process safely read a buffer it has received? When must it stop writing before handing it off? When, exactly, *is* the buffer handed off?

We therefore take the concept of *ownership* as our primitive abstraction, and base our formal invariants¹ on the following four properties that must hold if an entity can really be said to “own” a thing:

1. A thing has at most one owner.
2. If an entity owns a thing, it has exclusive use of it.
3. An entity knows whether it owns a thing or not.
4. Ownership can be transferred.

From the first property we infer the fundamental invariant of the model:

$$O_A \cap O_B = \emptyset$$

The set of things owned by A (O_A) is disjoint from the set of things owned by B (O_B), for any processes A and B . Note that a process is anything that might read or modify a buffer: a user-space process, a device driver, a hardware component (e.g. a network card).

The second property expresses the most important guarantee that the system must provide to processes (and that processes must, in turn, respect): First, if A owns a buffer, any changes to the buffer visible to A must be due to modifications A itself made since gaining ownership; Second, no other process (B) may rely on the contents of the buffer until A relinquishes ownership and B acquires it; Third, all changes caused by A (while it owned the buffer) must be visible to B *immediately upon acquiring ownership*. This guarantees isolation among processes, and provides clear requirements for any code needing to manage a weak or non-coherent memory system (by dictating barriers, flushes, etc. see Section 3.4).

The third and fourth properties force us to elaborate the formal model: If atomic transfer were possible, we could stick with just the sets by A and B and the bookkeeping problem would be straightforward. Generally however, no atomic transfer of ownership is possible: most implementations (especially hardware) transfer buffers by means of a descriptor ring or similar. The relinquishing process enqueues a descriptor referring to the buffer to be transferred, which the acquiring process (eventually) dequeues.

Note that the transfer sets (Q_{AB} and Q_{BA}) at this point do not preserve ordering. We add the FIFO property by refining the model in section 3.2.

While a buffer is in the queue (descriptor ring), it *cannot* be said to belong to either A or B in a way compatible with our 4 properties. If the buffers queued from A to B (Q_{AB}) belong to A , A is free to modify them as it likes (property 2). But as soon as the descriptor is dequeued, B will assume it owns it (e.g. the NIC will start writing). As enqueue and dequeue are asynchronous, A has no way of knowing when to stop writing! Likewise, assigning ownership of Q_{AB} to B violates property 3: B gains ownership (and thus responsibility) without being informed (when A enqueues). The queues are therefore distinct

¹Properties that must *always* hold.

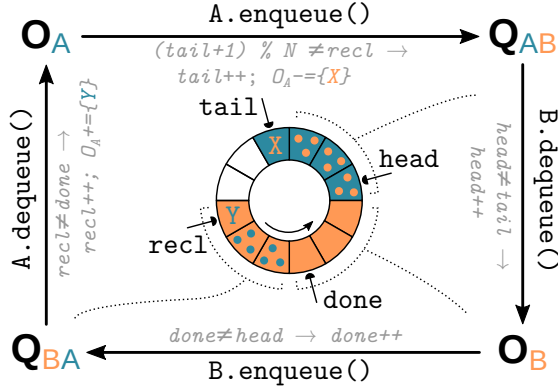


Figure 2: Ownership in the i82599 ring buffer

from the ownership sets (and from each other):

$$\begin{aligned} O_A \cap Q_{AB} &= O_B \cap Q_{AB} = \emptyset \\ O_A \cap Q_{BA} &= O_B \cap Q_{BA} = \emptyset \\ Q_{AB} \cap Q_{BA} &= \emptyset \end{aligned}$$

This is the complete model, illustrated by Figure 1. Here we see the four sets describing the transfer of ownership between processes A and B, and the allowable transitions. Barring `A.register()` and `B.register()` (which add buffers to, and remove them from bookkeeping), the four operations (`A/B.enqueue()`, `A/B.dequeue()`) transfer ownership of buffers clockwise: $O_A \rightarrow Q_{AB} \rightarrow O_B \rightarrow Q_{BA} \rightarrow O_A$.

One final invariant completes the model, and expresses that buffers are never lost, or invented out of thin air:

$$O_A \cup Q_{AB} \cup Q_B \cup Q_{BA} = \text{CONST}$$

3.1. Modelling the Intel i82599 Descriptor Ring

Figure 2 illustrates the descriptor ring buffer of the Intel i82599 10GbE network controller [29, 27] used in Intel’s popular X520 server network cards, and how it is interpreted in the CleanQ model. The ring itself (figure center) is a circular buffer with two pointers: `head` and `tail`. The descriptors from `head` up to (but not including) `tail` are those enqueued but not yet taken by the device i.e. the set Q_{AB} (here A is the driver and B the NIC).

The driver enqueues `X` by writing at `tail`, then incrementing the pointer, atomically transferring `X` from O_A to Q_{AB} . The NIC dequeues by incrementing `head`, atomically moving a buffer from Q_{AB} to O_B , (`done` up to `head`). The `done`² pointer is only modified by hardware and points to the last (oldest) buffer that the NIC has dequeued but not yet processed.

Only `tail`, `head` and `done` have hardware-dictated meaning — The NIC doesn’t distinguish (and doesn’t need to) between buffers that are enqueued back to the driver (Q_{BA}) and already dequeued in software and ready for reuse (unshaded

²There are two hardware modes: An *explicit* `done` pointer, or a `done` bit in the descriptor which defines an *implicit* `done` pointer

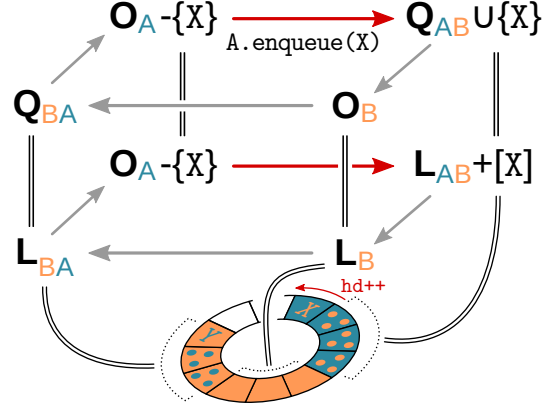


Figure 3: Refinement steps

descriptors in Figure 2). The driver keeps track of which descriptors it has dequeued (and are safe for reuse), with the `recl` pointer. This points to the oldest descriptor in Q_{BA} (the last shaded). The i82599 processes buffers in order. `recl` divides the region between `tail` and `done` into the returned descriptor queue (Q_{BA}) (`recl` to `done`) and ‘free’ descriptors (`tail` to `recl`).

All four of the queue operations consist of atomically incrementing a pointer (as indicated in gray in Figure 2, together with the guards (\rightarrow) against letting the head of a queue overtake its tail).

This shows that the CleanQ specification and its notion of ownership do, in fact, model the i82599 hardware queues – CleanQ closely corresponds to the design of real, high-performance hardware. The extremely simple implementation possible in this case also demonstrates that there is no inherent overhead to a well-specified formal interface, such as CleanQ.

O_A (the buffers owned by A) cannot be defined by the content of the descriptor ring. A might have e.g. `register`-ed a pool of buffers, shared between multiple queues. Operations on O_A are thus defined abstractly:

$$\begin{aligned} \text{A.enqueue}(X) &: O_A := O_A - \{X\} \\ \text{A.dequeue}(Y) &: O_A := O_A \cup \{Y\} \end{aligned}$$

Any *implementation* of `A.enqueue()` must cause A to relinquish ownership of `X` and that of `A.dequeue()` cause A to take ownership of `Y`. This is not a property on the ring buffer, but rather a correctness requirement for software that *uses* the ring buffer: It tells the programmer exactly *when* they must relinquish ownership, and exactly when they may assume they have re-acquired it.

3.2. Refinement

This notion of a ‘specification to be implemented’ is a *data refinement* (as used e.g. in the seL4 proof [5, 47]), and is also how our i82599 interpretation is formally specified. Figure 3 depicts a stepwise refinement of `A.enqueue(X)` from the abstract set-based model described so far, via an intermediate

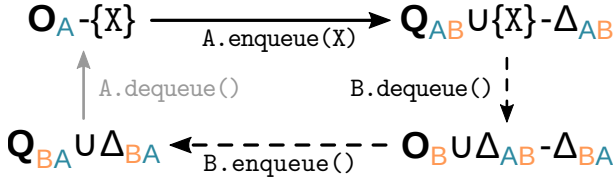


Figure 4: Weak postconditions for concurrency

model where queues become *lists* (establishing FIFO order), to the ring buffer model just described.

Each layer is the ownership transfer ring (c.f. Figure 1) at a given refinement level. Double lines indicate elements linked by the *state relation* e.g. the set Q_{AB} contains exactly the elements of the *list* L_{AB} which is in turn the descriptors from done up to head in the ring. Red arrows highlight the refinement of $A.\text{enqueue}(X)$, from set insertion ($Q_{AB} \cup \{X\}$) to list append ($L_{AB} + [X]$) and finally pointer increment ($\text{head}++$).

The state relations, and refined datatypes and operations are all formalised in Isabelle/HOL. Following the convention used in Formal Methods conferences, we do not include them here for space reasons, but all Theory sources will be published and are available on request.

3.3. Concurrency

CleanQ is fully concurrent, and mandates no locks. A and B may simultaneously enqueue and dequeue to their shared queues, as long as the invariants are preserved. For the i82599 this reflects that, for example, head is updated by the NIC obliviously to everything except that it does not overtake tail . The driver is free to enqueue at tail at precisely the moment that the NIC dequeues at head .

The *strict postconditions* of Figure 3 are not preserved by the actions of a concurrent process. For example, the strict postcondition $Q_{AB}^{\text{new}} = Q_{AB}^{\text{old}} \cup \{X\}$ for $A.\text{enqueue}(X)$ is invalidated if B dequeues X .

In reasoning about A , we cannot rely on X being in Q_{AB} , just because A has executed $\text{enqueue}(X)$. We *can*, however, infer that X is in one of Q_{AB} , O_B or Q_{BA} — everywhere B might have put it, without A doing anything (i.e. calling dequeue). Figure 4 summarizes the *weakened* postcondition for $\text{enqueue}(X)$ that is preserved under *interference* by B .

These weakened postconditions are a prerequisite for verifying the correctness of a particular implementation under full concurrency, using Owicki-Gries [36] logic as, for example, in the verification of the eChronos real-time operating system [2]. We have formalized these, also in Isabelle/HOL, including noninterference and refinement proofs for all abstract levels.

3.4. Caches and Memory Fences

Knowing exactly when ownership is gained and lost is essential to knowing exactly which *cache management operations* and *fences/barriers* are needed, and when, in order to correctly provide the guarantees implied by our ‘four properties of ownership’. In particular, weak-memory-model architectures (such

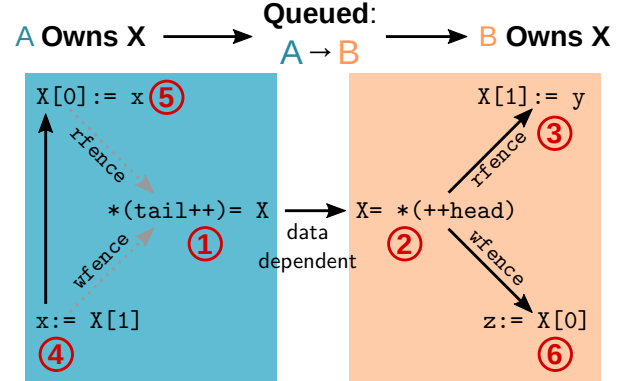


Figure 5: Ownership implies fences

as ARM and Power [34]) and partially- or non-coherent systems (e.g. accelerators) may violate the exclusivity guarantees by reordering memory operations past the ownership transfer (by reordering or speculatively executing instructions, or by serving stale values from non-coherent caches).

Consider Figure 5, depicting the transfer of the buffer X between sender A and receiver B , on a hypothetical very-weak-memory architecture (similar situations are or were observable on IBM Power and DEC Alpha systems). In the absence of fences (barriers), the only orderings guaranteed are those with a data dependency, marked with a solid arrow. The two dotted arrows between A ’s modifications to the buffer and its relinquishing ownership (incrementing tail) only indicate the *intended* ordering; These operations may occur in any order. In particular, the execution order indicated by the circled red numbers is consistent with the constraints (and can actually be observed).

Here we see A relinquish ownership (1), then B acquire it (2) and immediately write value y to $X[1]$ (3). Only *then* are A ’s modifications scheduled: It reads the value in $X[1]$ (y , at 4), and writes it into $X[0]$ (5). Finally, B reads the value in $X[0]$, and sees the value y that it itself wrote. B has communicated to itself by traveling into the ‘past’!

A sufficient fix in this case is to add the read and write fences as indicated. A ’s read from $X[0]$ is forced to commit before the increment to tail (as it also involves a read), and likewise the write to $X[1]$. The read and write fences in B are redundant in this example (as in fact is A ’s write fence due to the data dependency). If not all instructions in A and B are known however, all four barriers are necessary.

Where the ownership model helps here is that all four barriers can be inferred from the guarantees and responsibilities of ownership: A must ensure that any writes to X become visible to B *before* B learns that it owns X (i.e. A ’s write to tail becomes visible to B). The *last* point at which A can ensure this (as B ’s dequeue is asynchronous) is when it enqueues X — Hence the write fence before updating tail . Likewise A must not rely on X after relinquishing ownership — Hence the read fence before the enqueue. An equivalent argument implies the

necessity of the fences on B 's side (e.g. in the absence of a data dependency).

Furthermore, it should be possible to *automatically* place the required fences, for some combination of a (possibly-stronger) memory model (e.g. ARM or TSO) and known code in A and B . Such automatic inference in code of similar complexity was demonstrated by Liu et. al. [33]

4. Interface and Implementation

In this section we describe the C interface we derive from the formal model in the previous section, together with a set of implementations (termed “modules”, following Unix Streams [42]) we have built and evaluated for inter-process communication and device drivers.

Figure 7 shows the software architecture. To show the applicability of CleanQ to different devices and other use-cases, we have implemented modules for an AHCI [30] storage host adapter, an Intel e1000 NIC [25], an Intel i82599 10Gb NIC [27], a Solarflare SFN5122F low-latency NIC [45], a network protocol stack implementing UDP/IP, a shared-memory inter-process queue, and a DPDK [28] module for the Intel i82599 10Gb NIC. We also implemented a debug module, which checks the interface contract at runtime. We describe the detail of the network stack and debug modules in section 4.2.

We have applied CleanQ in Linux, DPDK, and a microkernel-based research OS, showing that it is deployable across multiple, complete existing systems. An additional, Rust-based implementation which exploits Rust's ownership-based type system is beyond the scope of this paper.

4.1. Definition

Figure 6 shows the C declarations for CleanQ. This interface is implemented by generic code which performs various integrity checks (such as region bounds for buffers) before calling corresponding module-specific methods in a vtable associated with the `struct cleanq` argument.

The `enqueue` and `dequeue` methods must adhere to their specification introduced in section 3. The additional `notify`, `register`, and `deregister` calls are described below.

We now describe the semantics of the CleanQ interface functions in detail. Interface calls that do not satisfy the required preconditions are bugs on the caller side and cause undefined behavior (though many are caught by the generic checking code). As in section 3, “process” denotes anything that changes buffers, for instance a software driver or the hardware of a network interface card.

Creation and destruction of queues is not part of the interface, since these processes are highly implementation specific and typically need module specific parameters, such as device registers of a network card, a shared memory buffer for the loopback/IPC queue, or another queue in case of the debug queue. Creating a queue must include initializing the `cleanq` data structure including the generic state and vtable.

Register takes a contiguous region of memory, previously owned by neither side of the queue, inserts it into the set of owned buffers, and returns an identifier for it to be used in subsequent enqueue and dequeue operations. Register is typically used in conjunction with buffer pools or slab allocators that allocate a large chunk of memory at once.

Register is of practical importance in cases where address-related state must be set up in advance, for example regions for RDMA-based transfers, or programming an IOMMU to make a region of memory accessible to both sides of the queue. In simple shared-memory cases it can be implemented as a null operation which returns the pointer address as the handle.

The `mem` argument is an OS-specific handle to a memory resource, e.g. a pointer to anonymous memory, a file handle to a mapped segment, or a capability to physical memory. The memory region has to be at least read-accessible from the calling process. At no time may the set of registered regions overlap with each other.

Deregister removes a previously-registered region with the supplied id from the queue. Deregister can only succeed if the region has not already been deregistered, *and* all memory in the region is currently owned by the calling process.

Enqueue enqueues a buffer of a previously registered region for ownership transfer. Buffers are identified by a region id, an offset into this region and a length. The buffer described by offset and length, must lie within the registered region, and must be owned by the process (i.e. a buffer cannot be enqueued twice without dequeuing it beforehand). The operation can fail if the underlying queue has run out of space.

The valid payload is specified by a further offset and length within the buffer, allowing clients to leave space for headers and footers (meta data) added later.

As specified, a successful enqueue relinquishes ownership of the buffer and inserts it into the transfer set. Eventually the ownership of the buffer will be obtained by the peer process, but there is no guarantee when this happens.

A client must not alter a buffer once it has given up ownership, and doing so will result in undefined behavior. Since we know precisely when we yield the ownership and which memory region is described by the buffer, the implementation can and must guarantee that all changes to the buffer are observable (using memory fences) before the ownership is transferred.

The `flags` field allows additional metadata to be passed along orthogonally with the buffer, with the proviso that the formal semantics from section 3 are not altered in any way. For example, a DMA copy engine might require the client to distinguish source and destination buffers for a copy.

Dequeue removes a previously enqueued buffer from the queue and transfers ownership of the buffer to the calling process. As long as the process owns a buffer, the process can alter the contents of this buffer. Dequeue can be called any time but returns an error if there is nothing to dequeue.

Absent an error, a correct implementation must return a

```

err_t cleanq_register(struct cleanq *q, void *mem, regionid_t* rid);
err_t cleanq_deregister(struct cleanq *q, void *mem, regionid_t rid);
err_t cleanq_enqueue(struct cleanq *q, regionid_t rid, size_t offset, size_t length,
                    size_t valid_data, size_t valid_length, uint64_t flags);
err_t cleanq_dequeue(struct cleanq *q, regionid_t* rid, size_t* offset, size_t* length,
                    size_t* valid_data, size_t* valid_length, uint64_t* flags);
err_t cleanq_notify(struct cleanq *q);

```

Figure 6: The CleanQ library interface

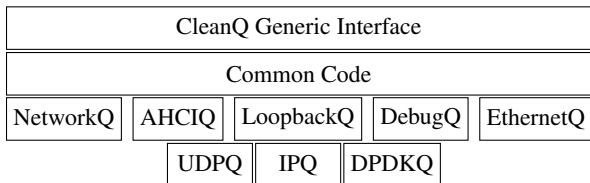


Figure 7: Implemented modules of CleanQ Library

valid buffer, i.e. one that is within a previously registered region and is not yet owned by the calling process. As with enqueue, a subset of the buffer can be declared valid using `valid_data` and `valid_length`, to allow stripping of headers (for example, in the UDP queue example we show in section 4.2).

Metadata about the transfer can, as with enqueue, be returned in `flags`. Again, this is implementation defined but must be orthogonal to the memory ownership semantics. It can be used to signal corrupt packets from a network adapter, for example, or as part of a chaining protocol (section 4.4)

Notify is an optional performance optimization mechanism: for example, a doorbell informing the process on the other side of the queue that there *might* (i.e. no guarantee) be buffers in the queue that are ready for processing. It has no formal semantics at all, and its use (or omission) must not affect the correctness of any implementation relative to the specification.

4.2. Module Composition and Debugging

We have implemented CleanQ modules which communicate with a variety of hardware devices using their native descriptor format and protocol, along with inter-process communication channels which pass descriptors in shared memory using a variant of FastForward [20]. Despite incorporating basic runtime checks, we show in Section 5 that these modules are comparable in performance with the “native” implementations they replace. However, CleanQ’s formally specified interface has a further advantage: in contrast to ad-hoc, C-specified queues, CleanQ modules can compose in a pipeline or stack, analogous to System V streams. The “null” implementation (a module which sits in front of another CleanQ module but simply passes data through) imposes negligible overhead, and we have implemented a *debug module* which augments CleanQ’s default bounds checks with more extensive bookkeeping to detect violations of the queue’s contract by either client or downstream module. For example, it maintains an operation log for debugging purposes, and detects overlapping or duplicate enqueues, which prevent “double fetch” race condition vulnerabilities [46].

4.3. Networking

We have built a full-duplex UDP protocol stack which sits atop a CleanQ module implementing a NIC’s hardware queues and which itself consists of two CleanQ modules: one for the UDP headers and one for IP and Ethernet headers. The result is a dataplane implementation similar to Arrakis [37]. The structure of the enqueue call is shown in figure 8. In order to

```

struct udp_q* que = ...
struct cleanq* q = (struct cleanq*) que;
cleanq_enqueue(q, ...){
    // Some interface checks
    q.enq(q, ...){
        // Build UDP header
        q->ip_q.enq(q->ip_q, ...){
            // Build IP + Ethernet header
            ip_q->nic_q.enq(ip_q->nic_q, ...){
                // Build descriptor and inform Hardware
            } } } }

```

Figure 8: Stacking queues to implement UDP

implement different layers of the stack, we use `valid_data` and `valid_length`. When receiving a packet, each layer reads and interprets the header found at offset `valid_data`. To pass a packet up to the next higher layer `valid_data` is incremented by the header size, such that the next higher layer will ignore the current layer’s header.

4.4. Discussion

Our experience building a number of CleanQ modules, and composing them, has so far been very positive. Implementation is generally straightforward, similar to a Virtio queue or an ad-hoc implementation, and establishes that the model is sufficiently general to cover all the use-cases we have encountered so far.

CleanQ’s formal semantics make it very clear what obligations exist for a module programmer at every point in the code, and remove most of the uncertainty about what the code needs to guarantee and when. The use of stackable modules provides the expected benefits in composability, and we have made extensive use of the debug module for checking.

Compared with other queue implementations in systems like Linux, however, CleanQ is something of a radical simplification, and this might raise several concerns.

Firstly, we are paying the price of abstraction: the clearer interface requires indirect method calls for each module. Historically these have been viewed as expensive, but as we show in Section 5 modern processors have reduced this overhead to

considerably less than the cost of, e.g., formatting hardware descriptors, and so this appears not to be an issue.

Secondly, each enqueue or dequeue operation acts on a single buffer: there is no batching. In practice, the cost of multiple enqueue/dequeue operations is sufficiently small in our implementations that this does not degrade performance significantly.

Finally, we do not directly support chaining of multiple, discontinuous buffers as with BSD `mbufs` or Linux `sk_bufs`. Instead, we chain buffers using a simple protocol *above* CleanQ’s single-buffer enqueue/dequeue operations. As with batching, the additional overhead is small for our usecases.

Our argument, backed up by performance measurements, is that the simplicity and rigorous semantics of CleanQ outweigh the small overhead the design might incur.

5. Evaluation

To evaluate the performance of CleanQ we first benchmark the overhead of our implementation of the interface, then compare the equivalent operations of Virtio to our queues. Following this, we set the overhead into perspective of a real application. We then further evaluate the different mechanisms of stacking, the debug queue and finish the performance benchmarks with a more complex example of an implementation of a UDP stack based on our queues as well as on DPDK. Finally we discuss the performance of CleanQ based on the previously presented benchmarks.

With these benchmarks we show that there is no significant performance loss when changing from existing systems to CleanQ while we gain a clean, easier to use, well-defined interface with the ability to stack queues. Furthermore, in our implementation of the interface we added sanity checks on the buffers through the thin library layer that are not included in most systems.

All experiments were conducted on a two-socket Intel Xeon E5-2670 v2 (Ivy-Bridge, 2.5 GHz) system with hyper threading disabled. We used an i8259-based Intel X520 dual-port 10GbE card to evaluate the performance of the UDP queue. Unless indicated otherwise, all measurements are taken using the timestamp counter of the processor. We evaluated CleanQ on Linux (Ubuntu 18.04 LTS) and a microkernel-based research OS.

5.1. The Overhead of Common Code

This benchmark shows that the performance overhead of our C implementation, which provides some sanity checks as common code, is small in absolute terms for all four operations *enqueue*, *dequeue*, *register* and *deregister*.

The benchmark setup is as follows: We configured CleanQ to use the *loopback*-module which resembles an in-memory ring buffer where enqueue writes the descriptor into memory and dequeue reads the descriptor contents from memory and the corresponding pointers are updated accordingly. We measure at two points: at the calls to the interface and the calls to

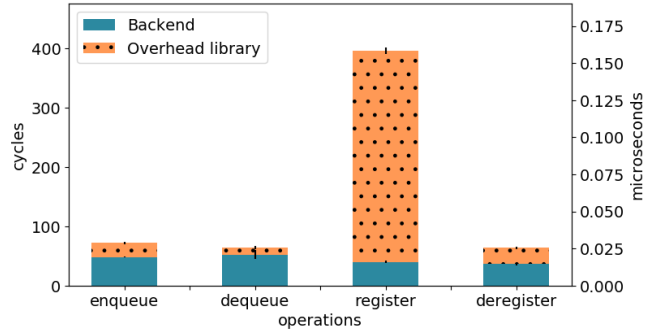


Figure 9: Overhead of C interface implementation

the module (before the `vtable` invocation). We run the benchmark of 100,000 repetitions and account for our measuring instrumentation.

Figure 9 shows the median (and standard deviation) of each of the four operations. We observe that the cost of the thin library layer of our CleanQ implementation is on the order of tens of cycles for the enqueue, dequeue and deregister operation whereas register requires an additional check that the memory region is actually owned by the caller resulting in about 400 cycles overhead for a system call and the required bookkeeping.

The results show that our implementation adds little overhead in exchange for a well-defined and clean interface based on a formal model. The overheads of the fast-path operations enqueue/dequeue are less than 30 cycles and require fewer cycles than the simple loopback module. We expect the register/deregister operations to be on the slow-path but nevertheless they only add a few hundred cycles at most for the bookkeeping operations.

5.2. Comparison with Virtio

In this benchmark we compare the operations of CleanQ (with our loopback module) that have an equivalent in Virtio (`add/get` vs. `enqueue/dequeue`) to show that the performance is comparable.

We compare CleanQ with Virtio (both on Linux) by measuring the calls to the application interface of CleanQ and Virtio’s `virtqueue` implementation. To measure the performance of Virtio we adapted one of the Linux Virtio tests, adding measurement code and increasing the number of repetitions. The Virtio test uses `virtqueue_add_inbuf()` to add buffers to the queue and after the host side has removed them, the buffers are reclaimed from the guest side by calling `virtqueue_get_buf()`. Note, the host side of the `virtqueue` is accessible through a *different* interface that requires a `memcpy` for adding data to the queue. For fairness we did not include the host side interface operations in this benchmark. The result of the benchmark is shown in Figure 10. Enqueueing a descriptor to the Virtio `virtqueue` costs 56 cycles while enqueueing a buffer through our interface and then

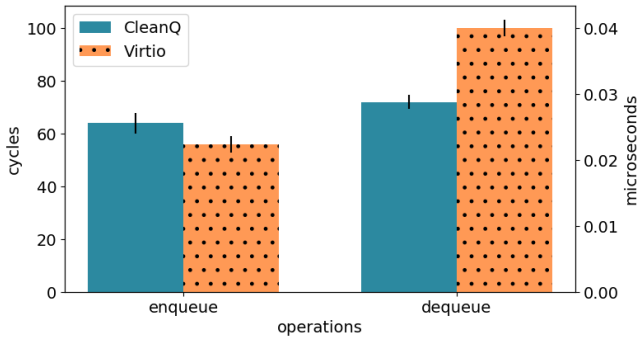


Figure 10: Performance of Virtio ring buffer (add/get) compared to CleanQ (enqueue/dequeue) both running on Linux

processing it in the module costs 72 cycles. Getting a descriptor from the virtqueue is more expensive at 100 cycles while dequeuing a buffer from CleanQ only costs 64 cycles.

Overall the performance is similar to Virtio’s guest side while CleanQ provides additional checks on the buffers, a cleaner and simpler interface that allows for more complex constructs by stacking queues on top of each other.

5.3. Placing library overhead in context

To put our C implementation overhead of CleanQ into perspective, we measure the total processing time of Memcached (v1.5.10) [17] including network stack and hashtable lookup for set and get requests. This is a simple application context in which CleanQ interface can be used.

We send small get/set requests (key + value < 16 bytes) over the network to our Memcached server. We profile incoming requests by measuring the network stack processing time and the duration of Memcached handling the get/set request. Note, the resolution of the software timestamps provided by the network stack is one microsecond (or 2500 cycles).

The results, in the form of a CDF plot of 100,000 set/get operations, are shown in Figure 11 for request handling in Memcached and Figure 12 for processing the packet in the network stack. The median time spent from the kernel to the userspace application on the receive path of a UDP packet is 3 microseconds or around 7500 cycles. The median of both set/get is around 3450 cycles (1.3 μ s). Combining these two measurements results in 10950 cycles (4.38 μ s) that are spent over the application’s path on which the CleanQ interface could realistically be used.

Comparing the time spent in the library on the fast path to the application’s time spent in other code, leaves the overhead of the library at < 1%. The small overhead of the library is dominated by the processing time of other parts of the code.

5.4. Module Stacking Overhead

In this experiment we measure the scalability of the implementations module stacking. We repeat the same experiment of section 5.1, but we now stack ten null modules on top of the loopback module. The null module mimics a no-op: it only

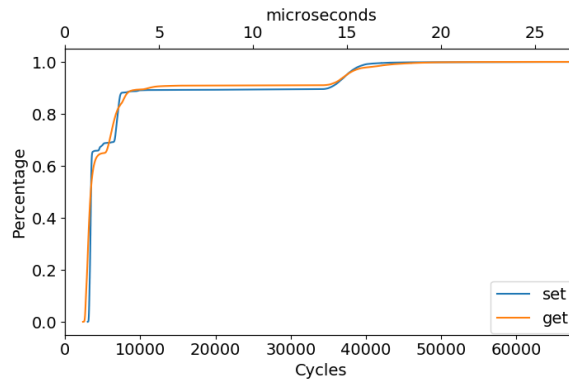


Figure 11: Memcached set/get processing time

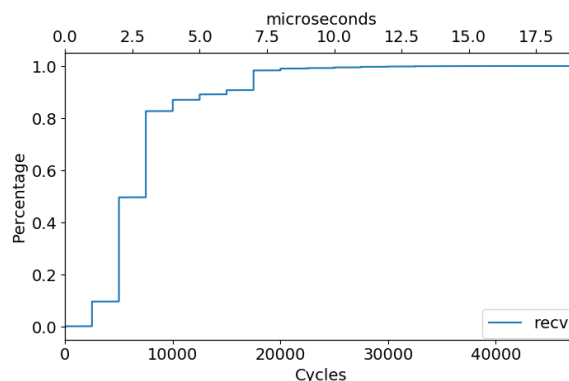


Figure 12: Linux: kernel to userspace network stack performance on receive path

invokes the same operation on the next module in the stack and therefore all observed overhead originates from stacking itself. We measure at different levels of the stack the time it takes until the lower level completes the operation. Again, we conducted 100,000 runs for each operation.

Figure 13 shows the median execution time and standard deviation at three different points of measurement: *i*) the base line (*loopback*) represents the lowest level of the stack which includes only the loopback module (corresponding to section 5.1) *ii*) *Null 1* represents the time taken when a single null module is stacked on top of the loopback module. We observe a negligible overhead for a single stack of less than 10 cycles for any of the operations. *iii*) *Null 10* measures the full stack of ten null modules stacked on top of the loopback module where the entire stack of ten modules results in about 100 cycles overhead compared to the baseline.

Each additional module stacked on top corresponds to an additional indirect function call, which results in the overhead of less than 10 cycles for stacking a single module. Moreover, our results suggest that the overhead per stacked module stays constant when more modules are stacked. With this experiment we have shown that CleanQ’s stacking functionality is efficient.

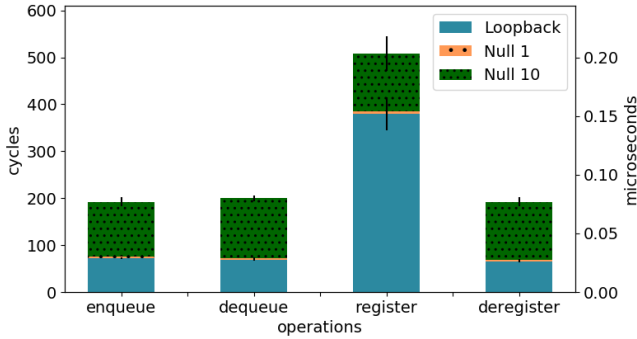


Figure 13: Overhead of stacking queues

5.5. Debug Module Overhead

In this experiment we measure the overhead of the debug module that performs additional checks of buffer ownership on every queue operation.

We repeat the experiment of section 5.1 with the only difference being that we stack the debug module on top of the loopback module. Again we perform 100,000 repetitions and measure the total execution time of each module in the stack.

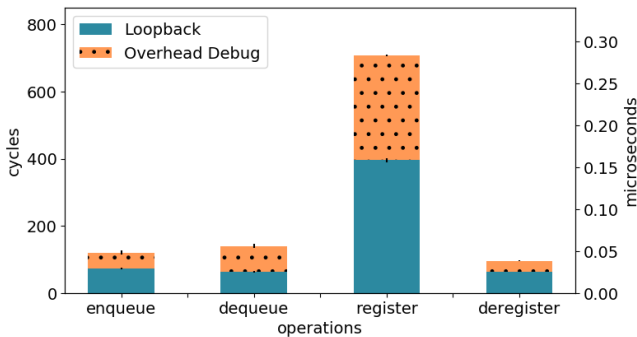


Figure 14: Overhead of debug queue

Figure 14 shows the median completion time for each operation including standard errors. We observe an overhead for the additional checks and stacking of the debug module of about 50-80 cycles for the enqueue and dequeue operations respectively and a total duration of 120-130 cycles. The deregister operation only adds about 20 cycles of overhead. Register is the most expensive operation adding 300 cycles.

The results show that even with tracking ownership, which requires lookup and updating internal data structures to reflect the change of ownership, we observe a total completion time for the two fast-path operations of less than 130 cycles. Deregister simply checks whether the region has been registered before and then removes it if all buffers are owned by the caller, resulting in low overhead. The register operation requires verifying the size and access rights which requires a syscall in our implementation, resulting in a 2x increase which is, however, still less than $0.3\mu s$

Putting the overhead of the debug into perspective, despite an increase of up to 2x relative to the loopback module, the

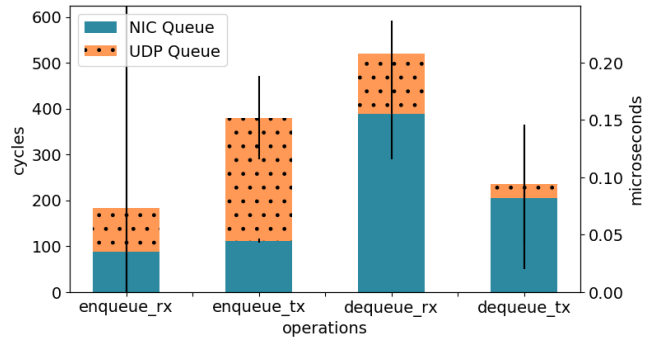


Figure 15: Performance of UDP queue

additional 50-80 cycles are dwarfed by the 3450 cycles processing time of our simple example application (Memcached) resulting in less than 2% overhead.

5.6. UDP Queue

In this benchmark we show that we can implement a more complex construct based on our stacking mechanism to realize a high-performance, low overhead UDP network stack similar to that in the Arrakis system [37]. This benchmark was implemented on the microkernel OS.

This benchmark consists of a UDP/IP echo server using CleanQ: a UDP module and an IP/Ethernet module both stacked on top of the e10k module which drives the Intel X520 dual-port 10GbE card. The resulting queue is a stack of three modules. The network card has a distinct queue for transmit and receive and for each of the two hardware queues we initialize a CleanQ stack. Note, the e10k module will need to convert from and to the descriptor format the network card understands. We generate 64-byte UDP packets and send them to the echo server with the CleanQ stack. We measure the processing time for sending and receiving the packet on the echo server.

Figure 15 shows the median and standard deviation based on 100,000 measured packets for the e10k module and the rest of the UDP network stack (Ethernet/IP/UDP) combined. We observe a much higher standard deviation compared to previous experiments.

On investigation, this latency distributed is heavily bimodal: the latency highly depends on whether the NIC hardware registers need to be updated. A write to the device register results in a 10x increase of the enqueue operation, but is only performed for a small fraction of enqueues. How frequently this expensive register write occurs depends on load and batching heuristics, but is inherent in the hardware and not a feature of CleanQ *per se*.

Enqueuing buffers into the transmit and receive queues of the NIC take about 90 cycles whereas processing the UDP module takes about 100-250 cycles. When a buffer is written into the hardware descriptor queue, the descriptor needs to be formatted which takes most of the 90 cycles. The work done by the UDP module includes growing the valid pointers

	Pkt/s	Standard deviation
DPDK	705,000	3362
CleanQ	713,100	7305
CleanQ UDP	742,600	5066

Table 1: DPDK vs. CleanQ vs. CleanQ UDP results

of the buffer to make space for the network headers as well as formatting the UDP, IP and Ethernet headers including the generation of checksums which account for the majority of the 250 cycles latency.

Dequeuing from the NIC queue is generally more expensive than enqueueing descriptors which result in 200-400 cycles latency. Dequeuing on the UDP module takes 20 cycles on the transmit queue and 120 cycles on the receive path. Whenever the NIC completes a descriptor it updates the status bit of the descriptor which in turn ends up in main memory or the last level cache introducing latency (90-150 cycles) when the descriptor is read by software. Moreover, the UDP module needs to verify the headers on the received descriptors.

To summarize, the performance characteristics of the hardware descriptor queues is generally dominated by the cost of formatting a descriptor and updating the register containing the receive and send pointers. Moreover, writing hardware registers to inform the card about the software state can be expensive (> 3000 cycles) and batching the updates can amortize the cost which is the source of the large variance in this experiment. We conducted similar experiments on a SolarFlare SNF5122F with comparable results.

Putting this into comparison of the library overhead, formatting a descriptor costs twice as much as our interface abstraction.

5.7. DPDK

In this benchmark we want to show that the CleanQ interface can also be integrated into existing systems without degrading performance.

We implemented a module based on the DPDK Intel ixgbe driver for the (i82599-based) Intel X520. We reuse the setup code and control plane of DPDK [28] but reimplement the dataplane as a CleanQ module. Additionally, we stacked the UDP stack on top of the NIC CleanQ module.

We compare the CleanQ module (and the UDP stack) to the original DPDK driver, measuring the packets per second of a single NIC queue using one core running a UDP echo server implemented using DPDK routines (send/recv burst). Furthermore, we also measure the performance of the CleanQ UDP stack directly using the CleanQ interface. To generate load we implemented a benchmark using standard sockets. On each core we run a thread which sends and receives the UDP packets in a closed loop with a configurable amount of packets in flight. Table 1 shows packets per second (median of 10 runs) using minimum-sized packets.

DPDK alone achieves a throughput of 705,000 pkts/s while DPDK using CleanQ achieved 713,100 pkts/s and the full UDP

stack using CleanQ reached 742,600 pkts/s. Incorporating the CleanQ interface into DPDK resulted in similar performance while implementing a UDP stack using only CleanQ increased performance by 5%.

This result shows that incorporating a CleanQ into a high-performance networking framework (DPDK) does not degrade throughput and can even deliver better performance.

5.8. Discussion

In the evaluation we demonstrated that CleanQ provides a clean and well defined queue abstraction with a strong notion of ownership transfer while still being lightweight (compared to full stack verification) and able to deliver comparable performance to Virtio’s virtqueue in a direct comparison. We have shown a C implementation of CleanQ with low overhead in absolute numbers as well as when used in an application context the resulting overhead to be less than 1% of the receive and processing time of Memcached get/set request. We further show that the overhead of CleanQ is not only dwarfed by application processing time but also by interfacing with the hardware itself such as by formatting descriptors and writing registers.

Furthermore, we have demonstrated CleanQ’s flexibility in building efficient protocols and adding strict bounds checks by stacking of modules – a feature which is enabled by the well defined abstraction of CleanQ. We have shown that stacking a module has a small overhead and is scalable to multiple modules. Finally, we have demonstrated this functionality by implementing a UDP network stack.

6. Conclusion

CleanQ demonstrates that it is possible to unify many of the proliferation of descriptor queues in common usage behind a single interface with strict formal semantics, at no performance cost on the dataplane.

The benefits begin with the elimination of many subtle bugs which appear (and reappear) whenever such an interface is defined informally. These include failing to catch all the usage cases, as well as different interpretations of the interface between client and implementation (which a strict formal specification prevents). The ownership-transfer model of CleanQ is sound under lock-free concurrency, and provides a framework for the verification of implementations.

The many CleanQ modules already implemented show that such an interface is widely applicable within an OS, and also permits the composition of modules to provide reuse of functionality.

Moreover, this generality, composability, and soundness come at a low cost: CleanQ matches Virtio for operation latency and imposes less than 1% overhead on end-to-end application workloads such as Memcached.

The Isabelle/HOL formalisations will be published separately as an extended technical report, and all CleanQ modules and support code will be released under an open source license.

References

- [1] Zach Amsden, Daniel Arai, Daniel Hecht, Anne Holler, Pratap Subrahmanyam, and VMware Inc. VMI: An Interface for Paravirtualization, 2006.
- [2] June Andronick, Corey Lewis, Daniel Matchuk, Carroll Morgan, and Christine Rizkallah. Proof of OS scheduling behavior in the presence of interrupt-induced concurrency. In Jasmin Christian Blanchette and Stephan Merz, editor, *International Conference on Interactive Theorem Proving*, pages 52–68, Nancy, France, August 2016. Springer.
- [3] Matias Björling, Jens Axboe, David Nellans, and Philippe Bonnet. Linux Block IO: Introducing Multi-queue SSD Access on Multi-core Systems. In *Proceedings of the 6th International Systems and Storage Conference*, SYSTOR '13, pages 22:1–22:10, Haifa, Israel, 2013. ACM.
- [4] Broadcom. *Standard Broadcom NetXtreme II Family Highly Integrated Media Access Controller*, October 2008. Revision PG203-R.
- [5] David Cock, Gerwin Klein, and Thomas Sewell. Secure Microkernels, State Monads and Scalable Refinement. In *Proceedings of the 21st International Conference on Theorem Proving in Higher Order Logics*, TPHOLs '08, pages 167–182, Berlin, Heidelberg, 2008. Springer-Verlag.
- [6] MITRE Corporation. CVE-2017-9986. <https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2017-9986>. November 2017.
- [7] CVE Details. CVE-2004-0555. <https://www.cvedetails.com/cve/CVE-2004-0555/>. July 2004.
- [8] CVE Details. CVE-2008-1317. <https://www.cvedetails.com/cve/CVE-2008-1317/>. March 2008.
- [9] CVE Details. CVE-2010-1187. <https://www.cvedetails.com/cve/CVE-2010-1187/>. Oktober 2010.
- [10] CVE Details. CVE-2015-1805. <https://www.cvedetails.com/cve/CVE-2015-1805/>. August 2015.
- [11] CVE Details. CVE-2015-5366. <https://www.cvedetails.com/cve/CVE-2015-5366/>. August 2015.
- [12] CVE Details. CVE-2015-7613. <https://www.cvedetails.com/cve/CVE-2015-7613/?q=CVE-2015-7613>. September 2015.
- [13] CVE Details. CVE-2016-5403. <https://www.cvedetails.com/cve/CVE-2016-5403/>. August 2016.
- [14] CVE Details. CVE-2016-7618. <https://www.cvedetails.com/cve/CVE-2016-7618/>. August 2017.
- [15] CVE Details. CVE-2017-14916. <https://www.cvedetails.com/cve/CVE-2017-14916/>. December 2017.
- [16] Peter Druschel and Larry L. Peterson. Fbufs: A High-bandwidth Cross-domain Transfer Facility. In *Proceedings of the Fourteenth ACM Symposium on Operating Systems Principles*, SOSP '93, pages 189–202, Asheville, North Carolina, USA, 1993. ACM.
- [17] Brad Fitzpatrick. Distributed Caching with Memcached. *Linux J*, 2004(124):5–, August 2004.
- [18] Shaked Flur, Kathryn E. Gray, Christopher Pulte, Susmit Sarkar, Ali Sezgin, Luc Maranget, Will Deacon, and Peter Sewell. Modelling the ARMv8 Architecture, Operationally: Concurrency and ISA. In *Proceedings of POPL: the 43rd ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages*, 2016.
- [19] Andrew Friedley, Torsten Hoefler, Greg Bronevetsky, Andrew Lumsdaine, and Ching-Chen Ma. Ownership Passing: Efficient Distributed Memory Programming on Multi-core Systems. In *Proceedings of the 18th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, PPOPP '13, pages 177–186, Shenzhen, China, 2013. ACM.
- [20] John Giacomoni, Tipp Moseley, and Manish Vachharajani. Fastforward for efficient pipeline parallelism: A cache-optimized concurrent lock-free queue. In *Proceedings of the 13th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, PPOPP '08, pages 43–52, New York, NY, USA, 2008. ACM.
- [21] Ronghui Gu, Zhong Shao, Hao Chen, Xiongnan Wu, Jieung Kim, Vilhelm Sjöberg, and David Costanzo. CertKOS: An Extensible Architecture for Building Certified Concurrent OS Kernels. In *Proceedings of the 12th USENIX Conference on Operating Systems Design and Implementation*, OSDI'16, pages 653–669, Savannah, GA, USA, 2016. USENIX Association.
- [22] Sangjin Han, Scott Marshall, Byung-Gon Chun, and Sylvia Ratnasamy. MegaPipe: A New Programming Interface for Scalable Network I/O. In *Proceedings of the 10th USENIX Conference on Operating Systems Design and Implementation*, OSDI'12, pages 135–148, Hollywood, CA, USA, 2012. USENIX Association.
- [23] Norman C. Hutchinson and Larry L. Peterson. The X-Kernel: An Architecture for Implementing Network Protocols. *IEEE Trans. Softw. Eng.*, 17(1):64–76, January 1991.
- [24] Intel Corporation. *Intel 82571 1 GbE Controller: Datasheet*.
- [25] Intel Corporation. *PCIe GbE Controllers Open Source Software Developer's Manual 631xESB/632xESB, 82563EB/82564EB, 82571EB/82572EI & 82573E/82573V/82573L*, 2009. Revision 2.3.
- [26] Intel Corporation. *Intel 82576 Gigabit Ethernet Controller Datasheet*, December 2010. Revision 2.61.
- [27] Intel Corporation. *Intel 82599 10 GbE Controller Datasheet*, December 2010. Revision 2.6.
- [28] Intel Corporation. Data plane development kit. <https://www.dpdk.org/>. August 2018.
- [29] Intel Corporation. Intel ethernet converged network adapter x520. <https://www.intel.com/content/www/us/en/ethernet-products/converged-network-adapters/ethernet-x520-server-adapters-brief.html>. August 2018.
- [30] Intel Corporation. Seiral ata advanced host controller interface (ahci) 1.3.1. <https://www.intel.com/content/www/us/en/io/serial-ata/serial-ata-ahci-spec-rev1-3-1.html>. August 2018.
- [31] Gerwin Klein, Kevin Elphinstone, Gernot Heiser, June Andronick, David Cock, Philip Derrin, Dhammika Elkaduwe, Kai Engelhardt, Rafal Kolanski, Michael Norrish, Thomas Sewell, Harvey Tuch, and Simon Winwood. seL4: Formal Verification of an OS Kernel. In *Proceedings of the ACM SIGOPS 22Nd Symposium on Operating Systems Principles*, SOSP '09, pages 207–220, Big Sky, Montana, USA, 2009. ACM.
- [32] Alexander Krizhanovsky. Linux Netlink Mmap: Bulk Data Transfer for Kernel Database. <http://natsys-lab.blogspot.com/2015/03/linux-netlink-mmap-bulk-data-transfer.html>. March 2015.
- [33] Feng Liu, Nayden Nedev, Nedyalko Prisdanikov, Martin Vechev, and Eran Yahav. Dynamic Synthesis for Relaxed Memory Models. In *Proceedings of the 33rd ACM SIGPLAN Conference on Programming Language Design and Implementation*, PLDI '12, pages 429–440, Beijing, China, 2012. ACM.
- [34] Luc Maranget, Susmit Sarkar, and Peter Sewell. A Tutorial Introduction to the ARM and POWER Relaxed Memory Models. 2012.
- [35] David S. Miller. How skbuffs work. Onlin., <http://vger.kernel.org/~davem/skb.html>.
- [36] Susan Owicki and David Gries. An axiomatic proof technique for parallel programs i. *Acta Inf.*, 6(4):319–340, December 1976.
- [37] Simon Peter, Jialin Li, Irene Zhang, Dan R. K. Ports, Doug Woos, Arvind Krishnamurthy, Thomas Anderson, and Timothy Roscoe. Arakis: The Operating System is the Control Plane. In *Proceedings of the 11th USENIX Conference on Operating Systems Design and Implementation*, OSDI'14, pages 1–16, Broomfield, CO, 2014. USENIX Association.
- [38] David Leo Presotto. Multiprocessor Streams for Plan 9. In *Proceedings of the United Kingdom UNIX User Group Summer Proceedings*, pages 11–19, 1993.
- [39] Realtek Semi-Conductor Co., Ltd. *RTL8029AS: Realtek PCI Full-Duplex Ethernet Controller with built-in SRAM*, January 1997.
- [40] RedHat. CVE-2015-9016. <https://access.redhat.com/security/cve/cve-2015-9016>. August 2015.
- [41] RedHat. CVE-2017-17381. <https://access.redhat.com/security/cve/cve-2017-17381>. November 2017.
- [42] D.M. Ritchie. A stream input-output system. *AT&T Bell Laboratories Technical Journal*, 63:1897–1910, 10 1984.
- [43] Rusty Russell. Virtio: Towards a De-facto Standard for Virtual I/O Devices. *SIGOPS Oper. Syst. Rev.*, 42(5):95–103, July 2008.
- [44] Peter Sewell, Susmit Sarkar, Scott Owens, Francesco Zappa Nardelli, and Magnus O. Myreen. X86-TSO: A Rigorous and Usable Programmer's Model for x86 Multiprocessors. *Commun. ACM*, 53(7):89–97, July 2010.
- [45] Solarflare Communications, Inc. *Solarflare SFN5122F Dual-Port 10GbE Enterprise Server Adapter*, 2010.
- [46] Pengfei Wang, Jens Krinke, Kai Lu, Gen Li, and Steve Dodier-Lazaro. How double-fetch situations turn into double-fetch vulnerabilities: A study of double fetches in the linux kernel. In *Proceedings of the 26th USENIX Conference on Security Symposium*, SEC'17, pages 1–16, Berkeley, CA, USA, 2017. USENIX Association.
- [47] S. Winwood, G. Klein, T. Sewell, J. Andronick, D. Cock, and M. Norrish. Mind the gap. In S. Berghofer, T. Nipkow, C. Urban, and M. Wenzel, editors, *Theorem Proving in Higher Order Logics (TPHOLs)*, volume 5674 of *Lecture Notes in Computer Science*, Berlin, Heidelberg, 2009. Springer-Verlag.